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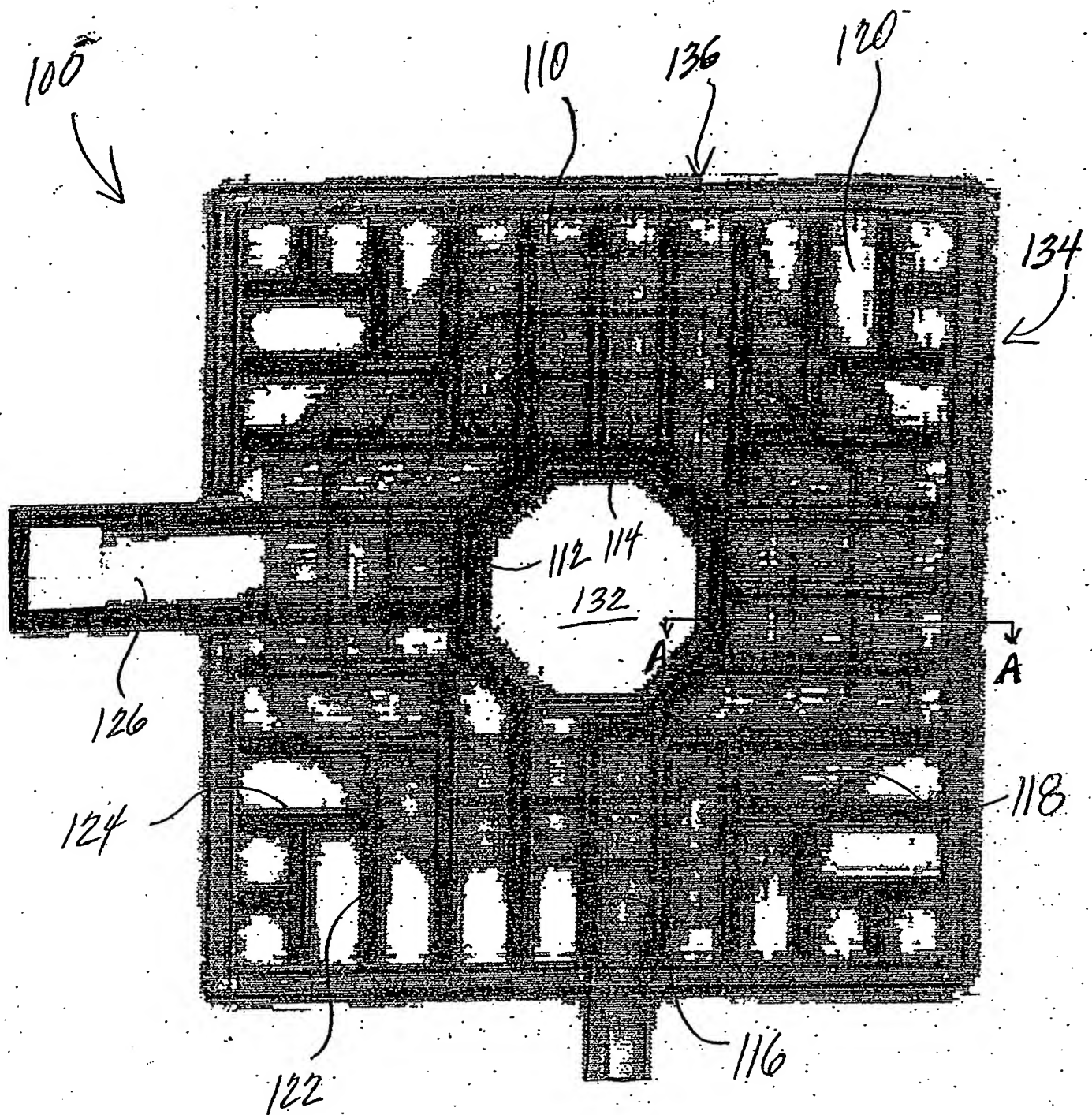


FIG. 1

200  
FORM FIRST DIELECTRIC LAYER OVER SEMICONDUCTOR SUBSTRATE

FORM FIRST MAGNETIC LAYER OVER FIRST DIELECTRIC LAYER

PATTERN FIRST MAGNETIC LAYER TO DEFINE AT LEAST ONE SLOT

FORM SECOND DIELECTRIC LAYER OVER FIRST MAGNETIC LAYER,  
FILLING EACH SLOT IN FIRST MAGNETIC LAYER

PATTERN SECOND DIELECTRIC LAYER  
TO DEFINE AT LEAST ONE VIA TO FIRST MAGNETIC LAYER

FORM CONDUCTIVE LAYER OVER SECOND DIELECTRIC LAYER

PATTERN CONDUCTIVE LAYER  
TO FORM A CONDUCTOR HAVING A SPIRAL-SHAPED SIGNAL PATH  
AND TO CLEAR ANY VIAS TO FIRST MAGNETIC LAYER

FORM THIRD DIELECTRIC LAYER OVER CONDUCTIVE LAYER

PATTERN THIRD DIELECTRIC LAYER  
TO DEFINE AT LEAST ONE VIA TO FIRST MAGNETIC LAYER

FORM SECOND MAGNETIC LAYER OVER THIRD DIELECTRIC LAYER,  
FILLING ANY VIAS TO FIRST MAGNETIC LAYER

PATTERN SECOND MAGNETIC LAYER TO FORM AT LEAST ONE SLOT

FIG. 2

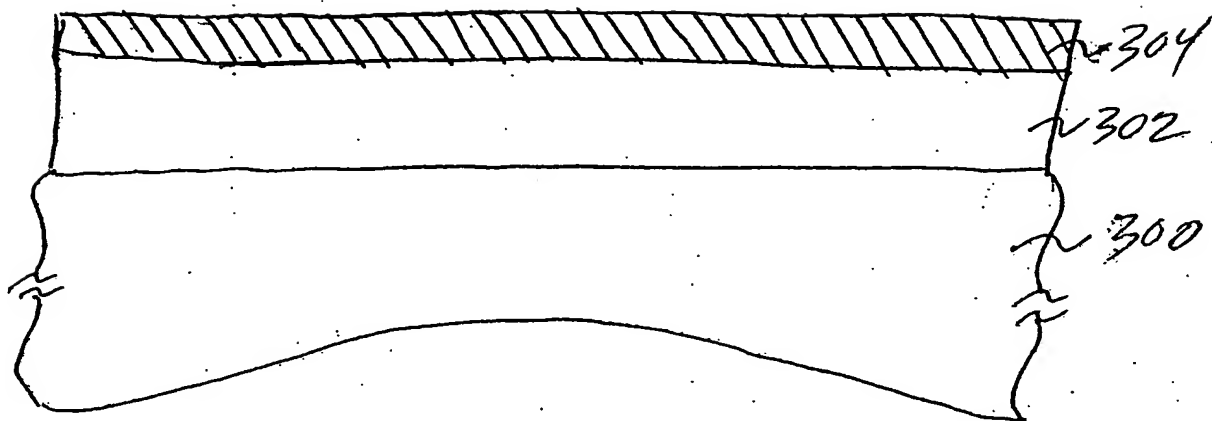


FIG. 3

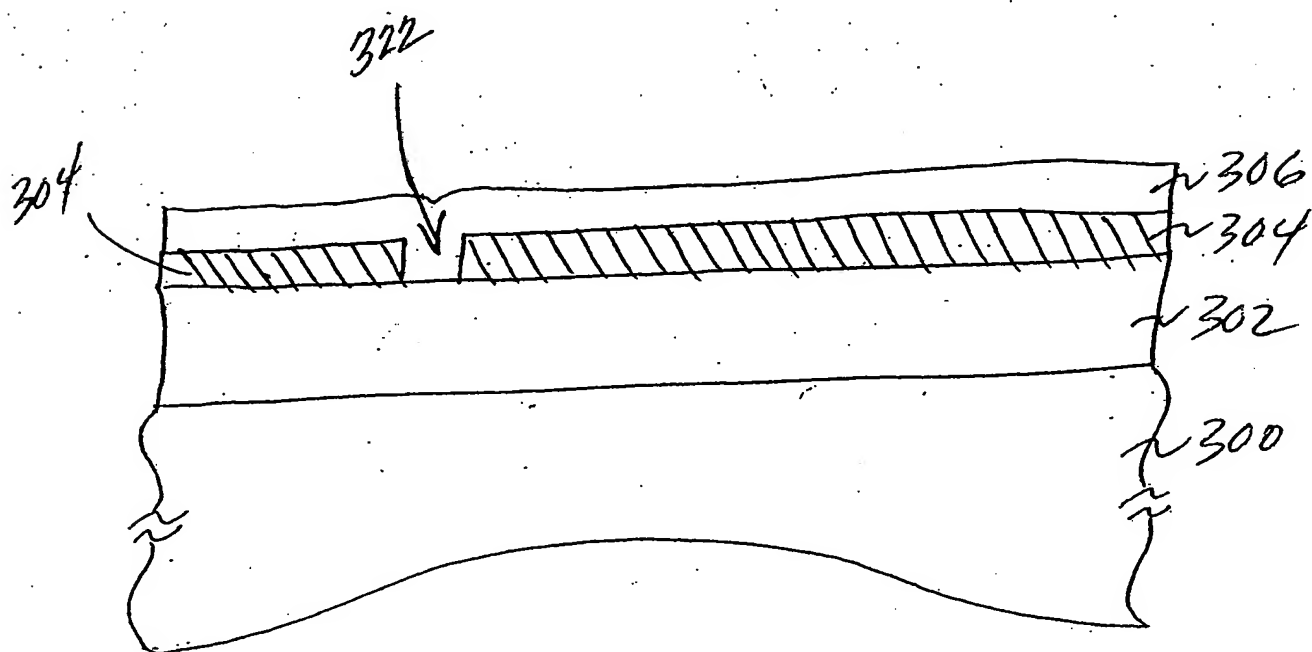


FIG. 4

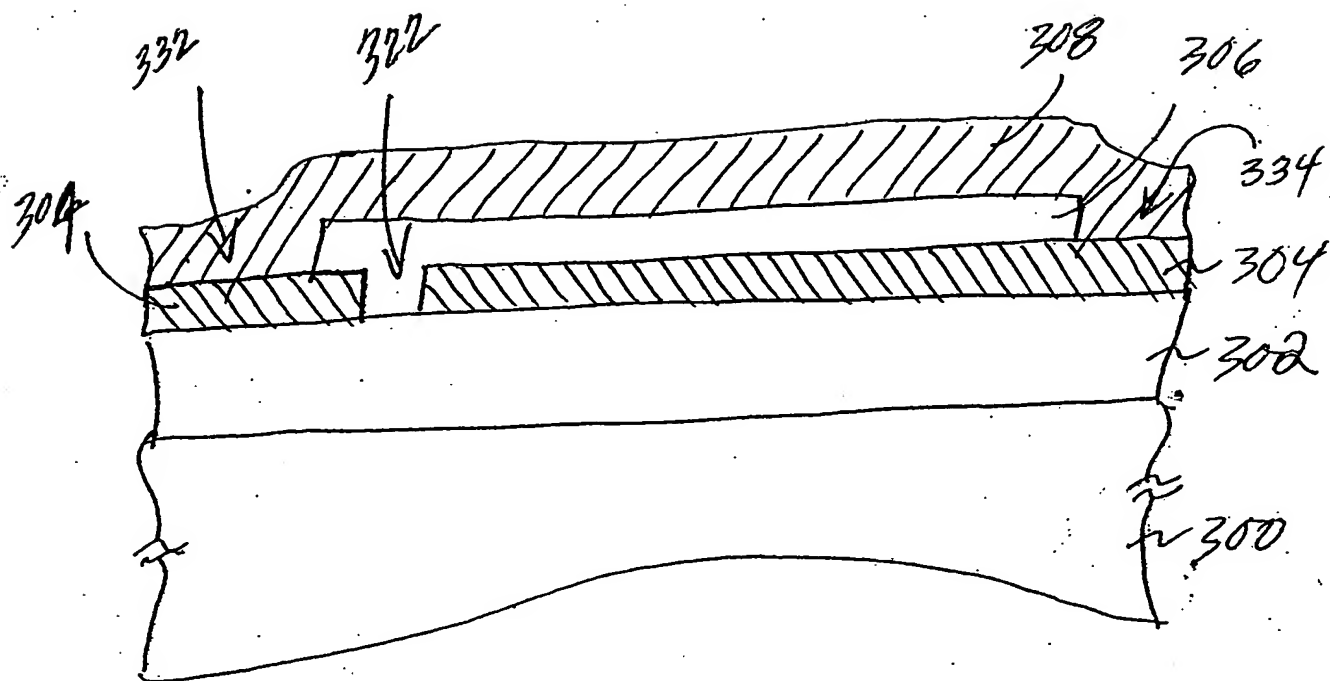


FIG. 5

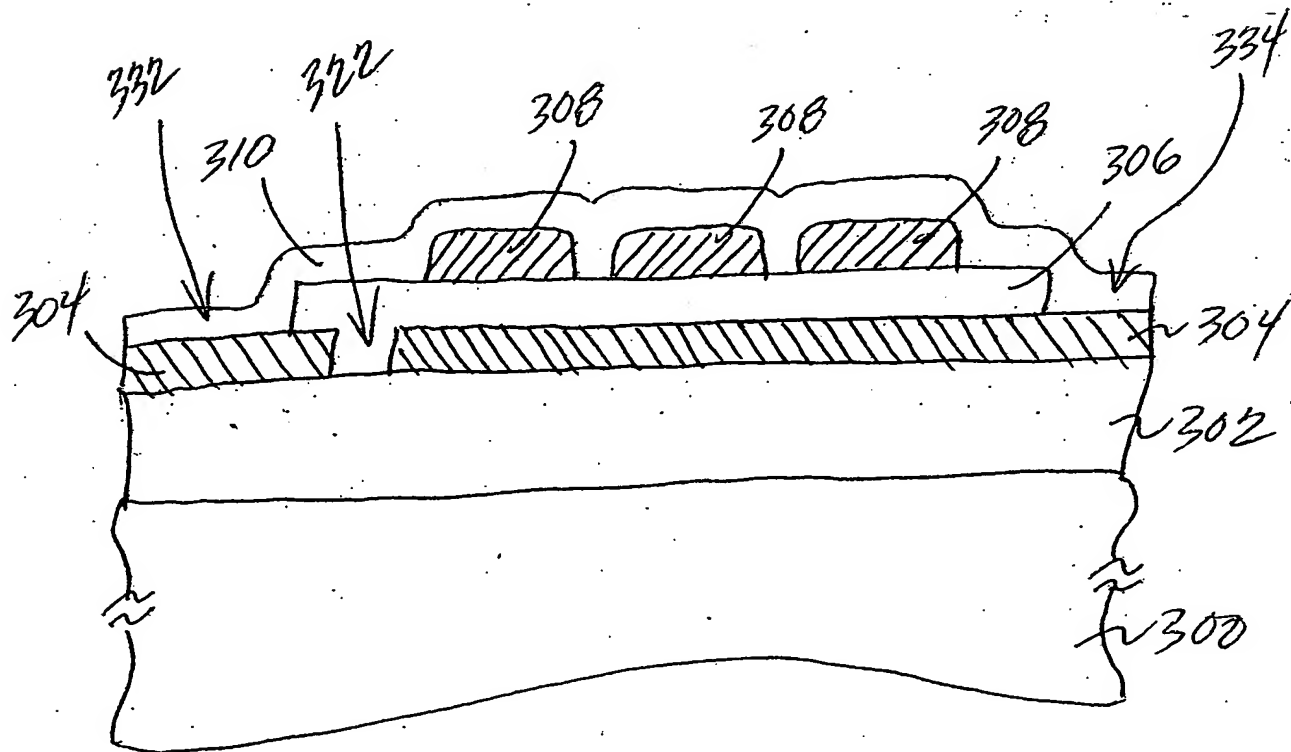


FIG. 6

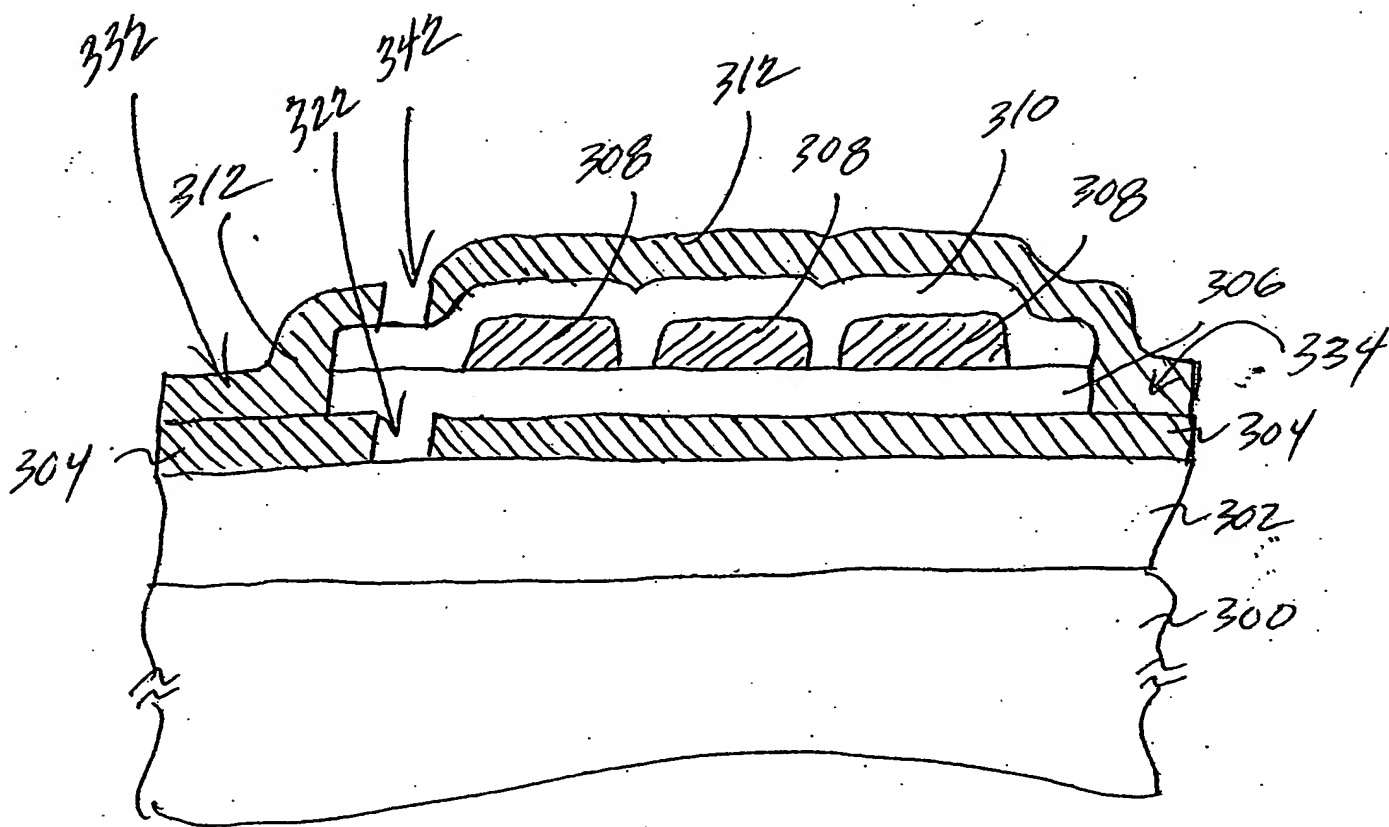


FIG. 7

900

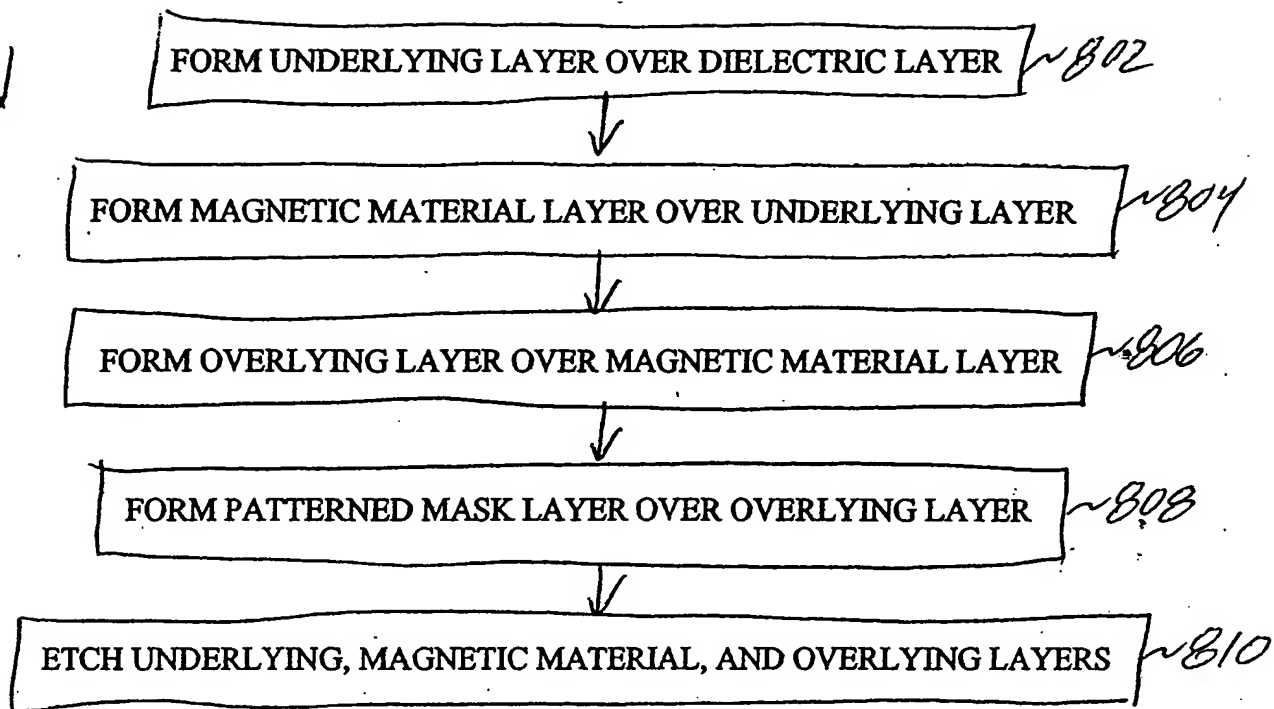


FIG. 8

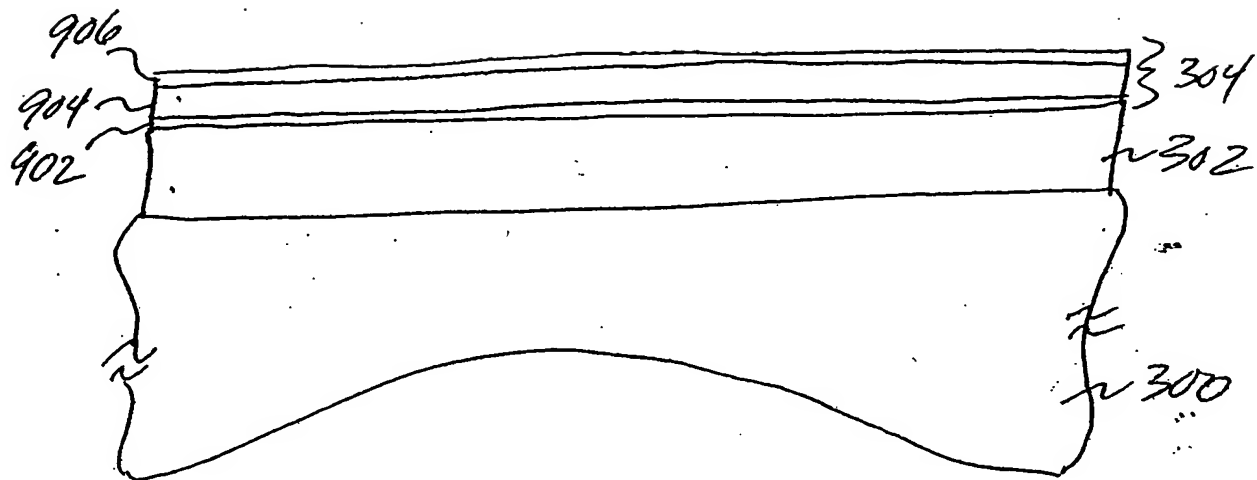


FIG. 9

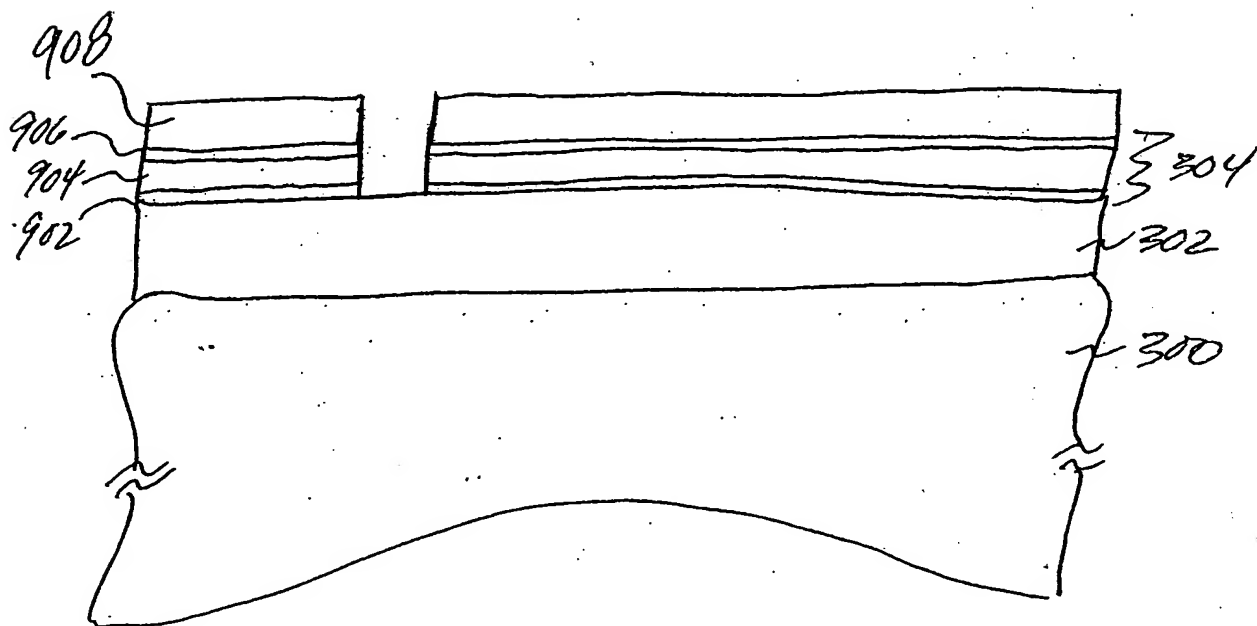


FIG. 10



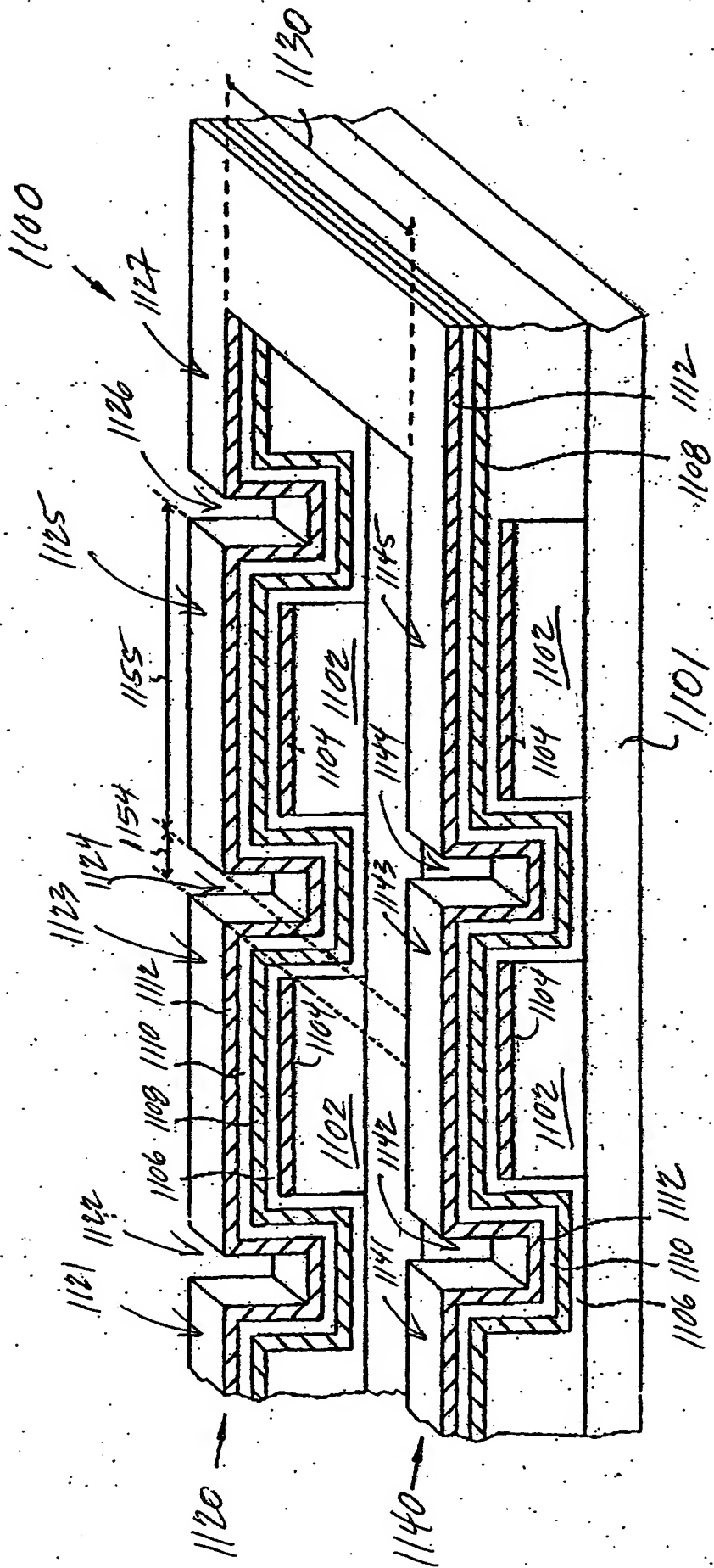


Fig. 11

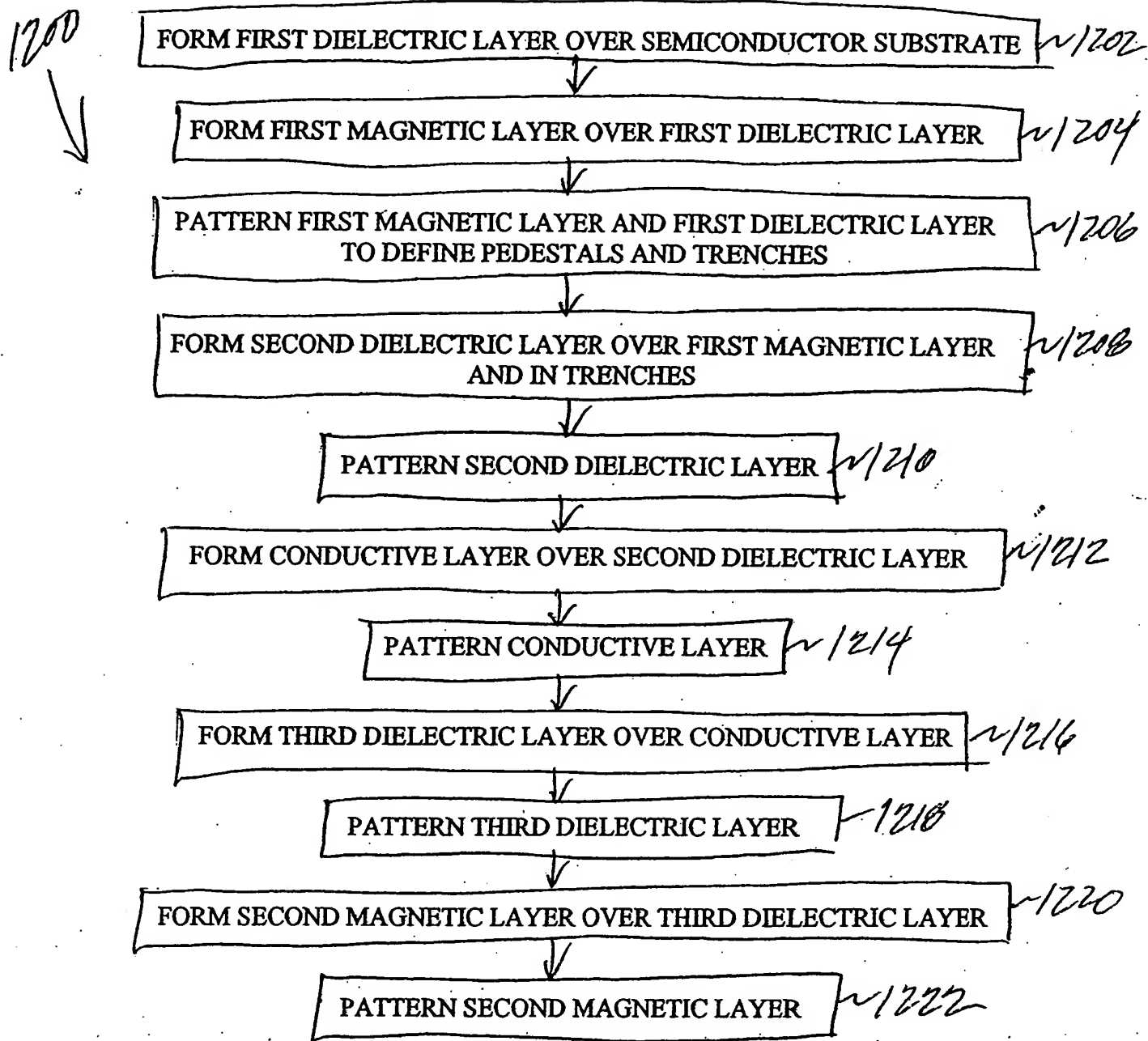


FIG. 12

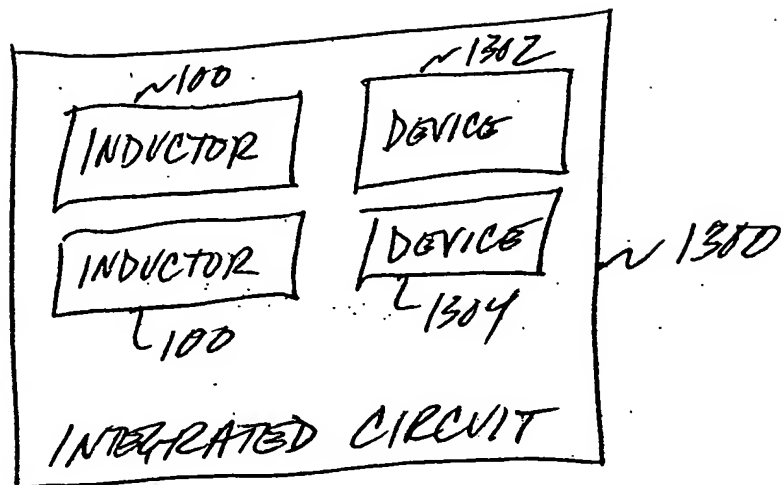


FIG. 13

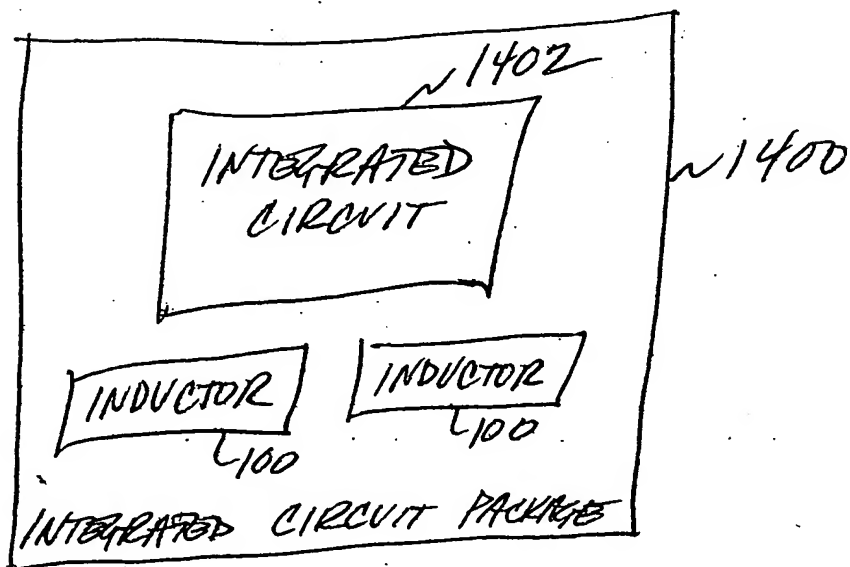


FIG. 14